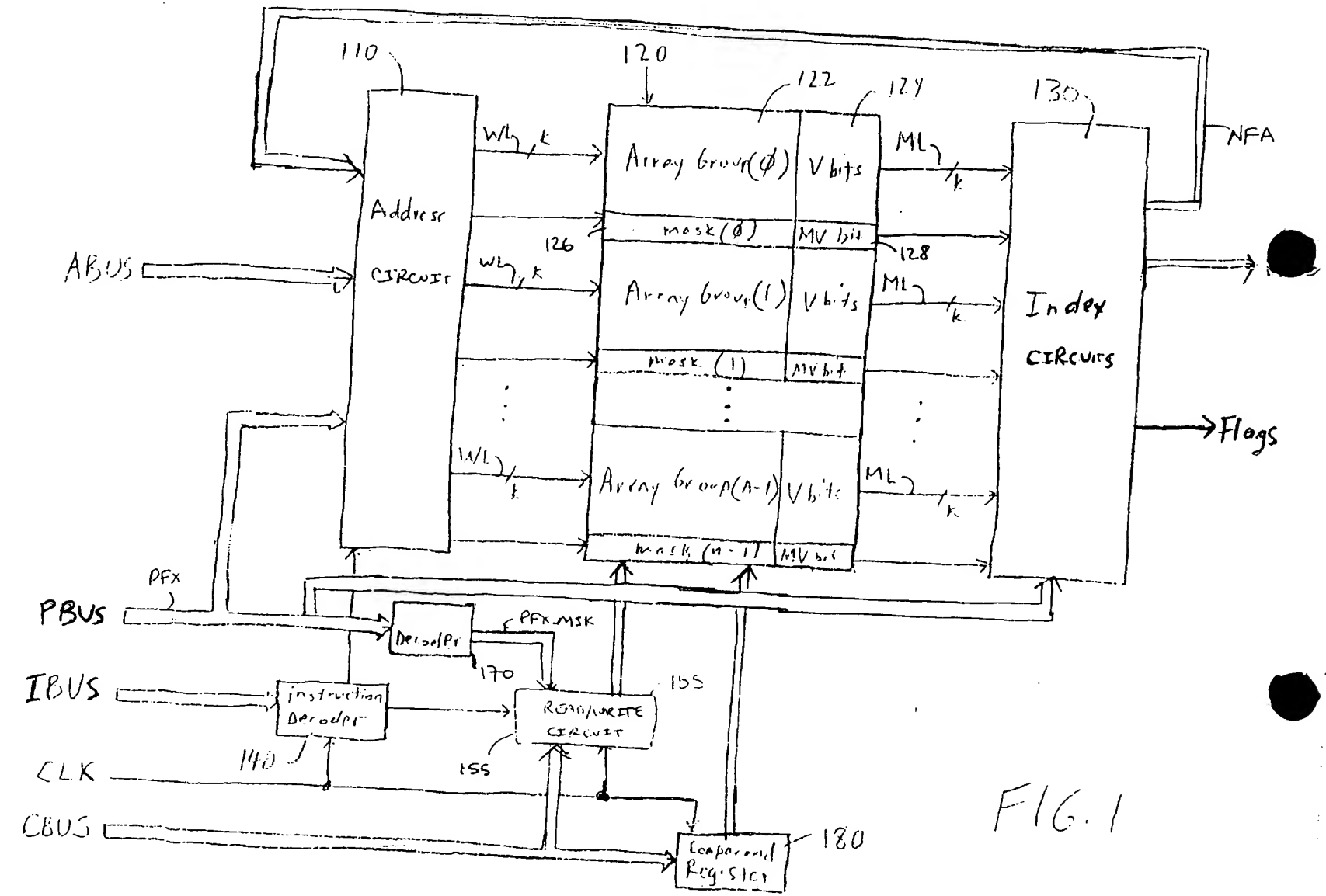

FIG. 1

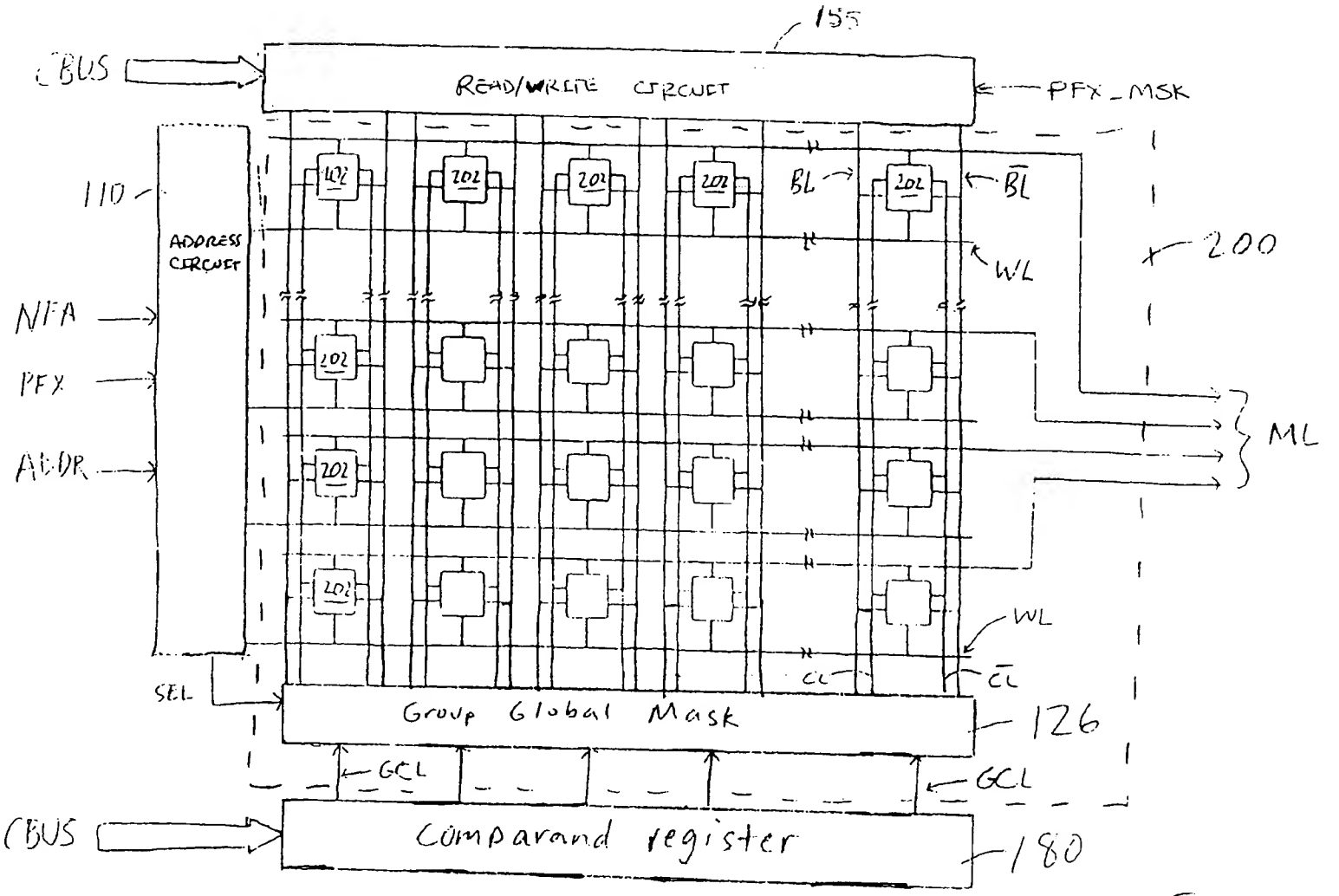

FIG. 2

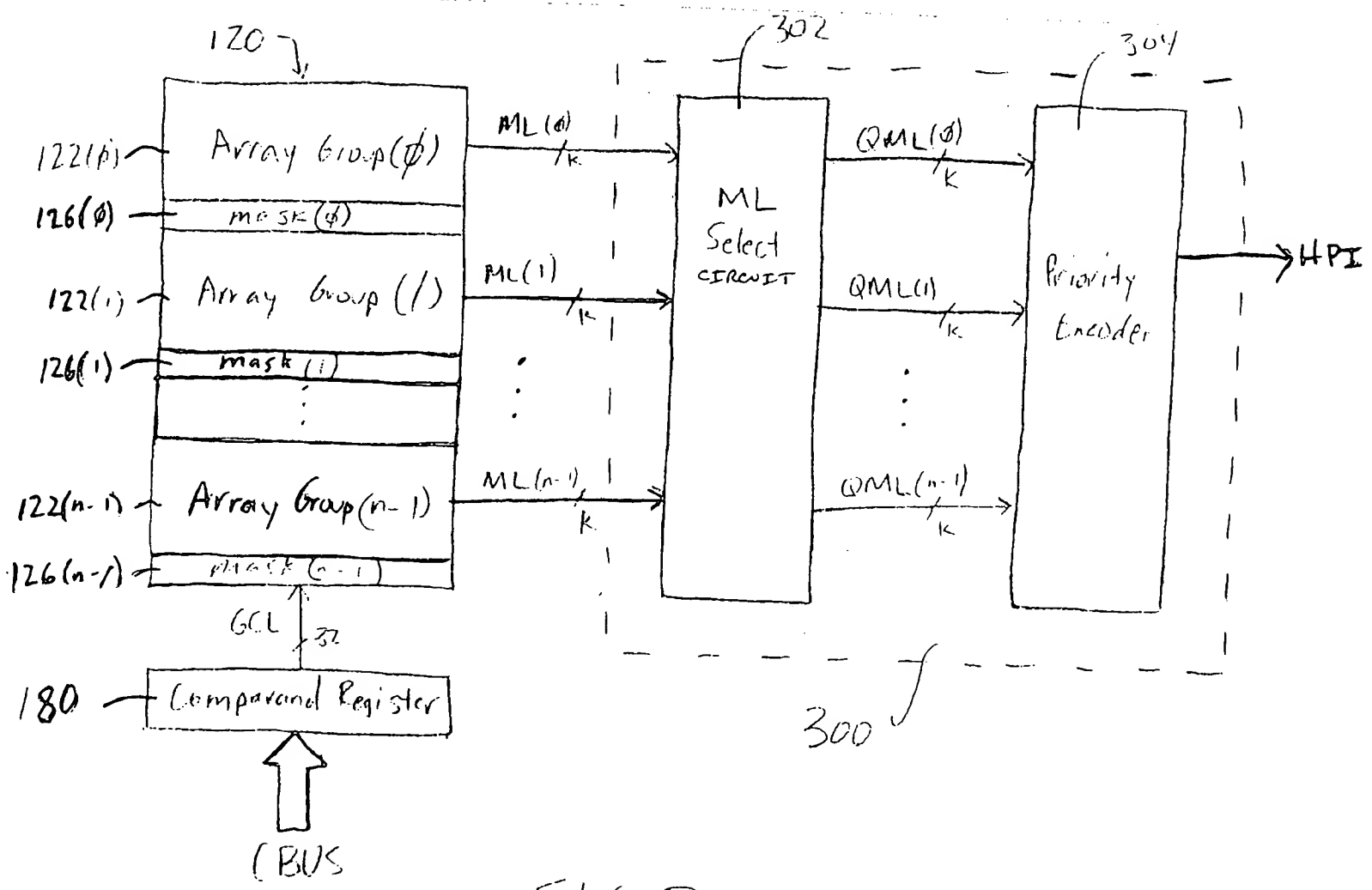

FIG. 3

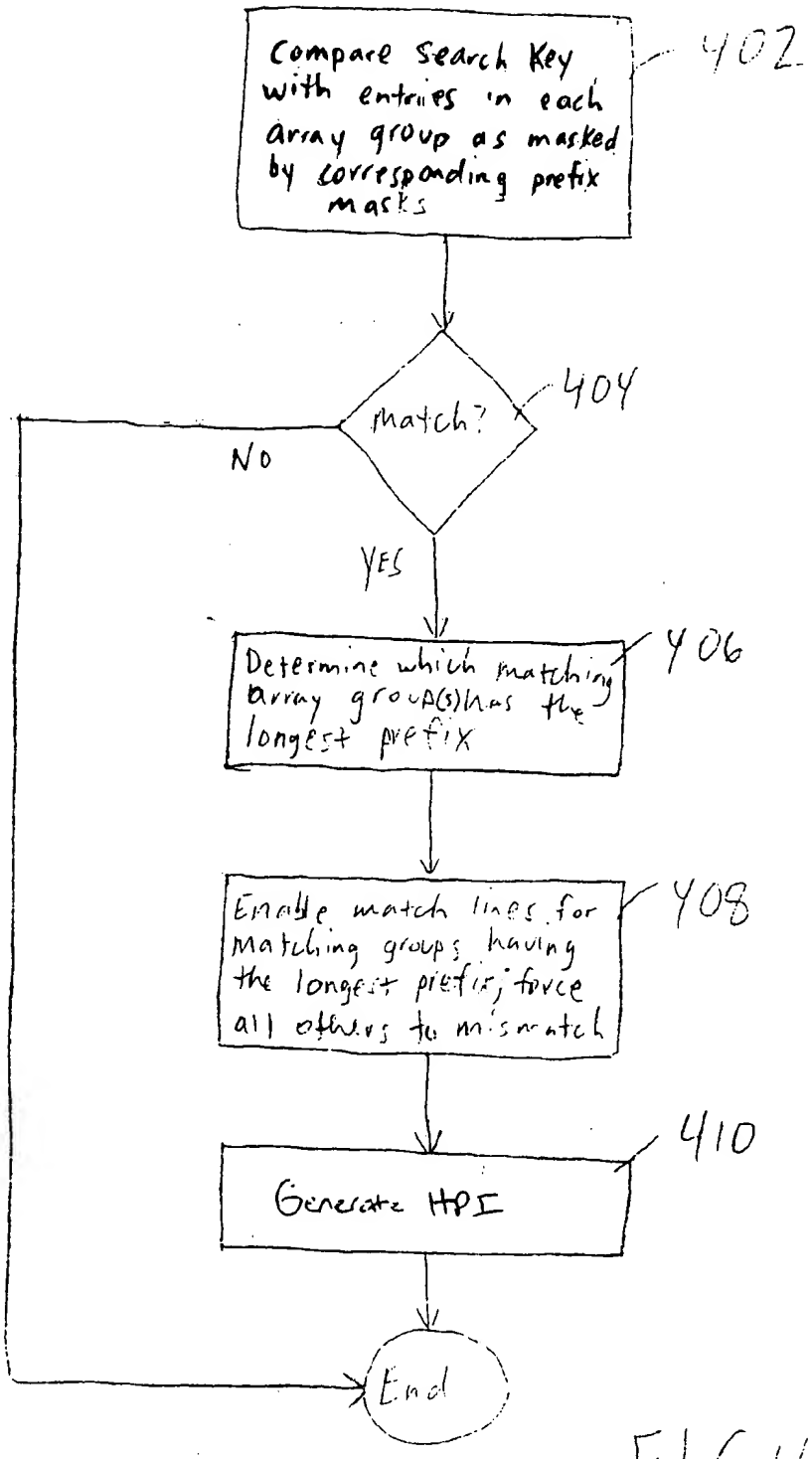
Compare Search Key with entries in each array group as masked by corresponding prefix masks
402
match?
404
NO
YES
Determine which matching array group(s) has the longest prefix
406
Enable match lines for matching groups having the longest prefix; force all others to mismatch
408
Generate HPI
410
End

FIG. 4

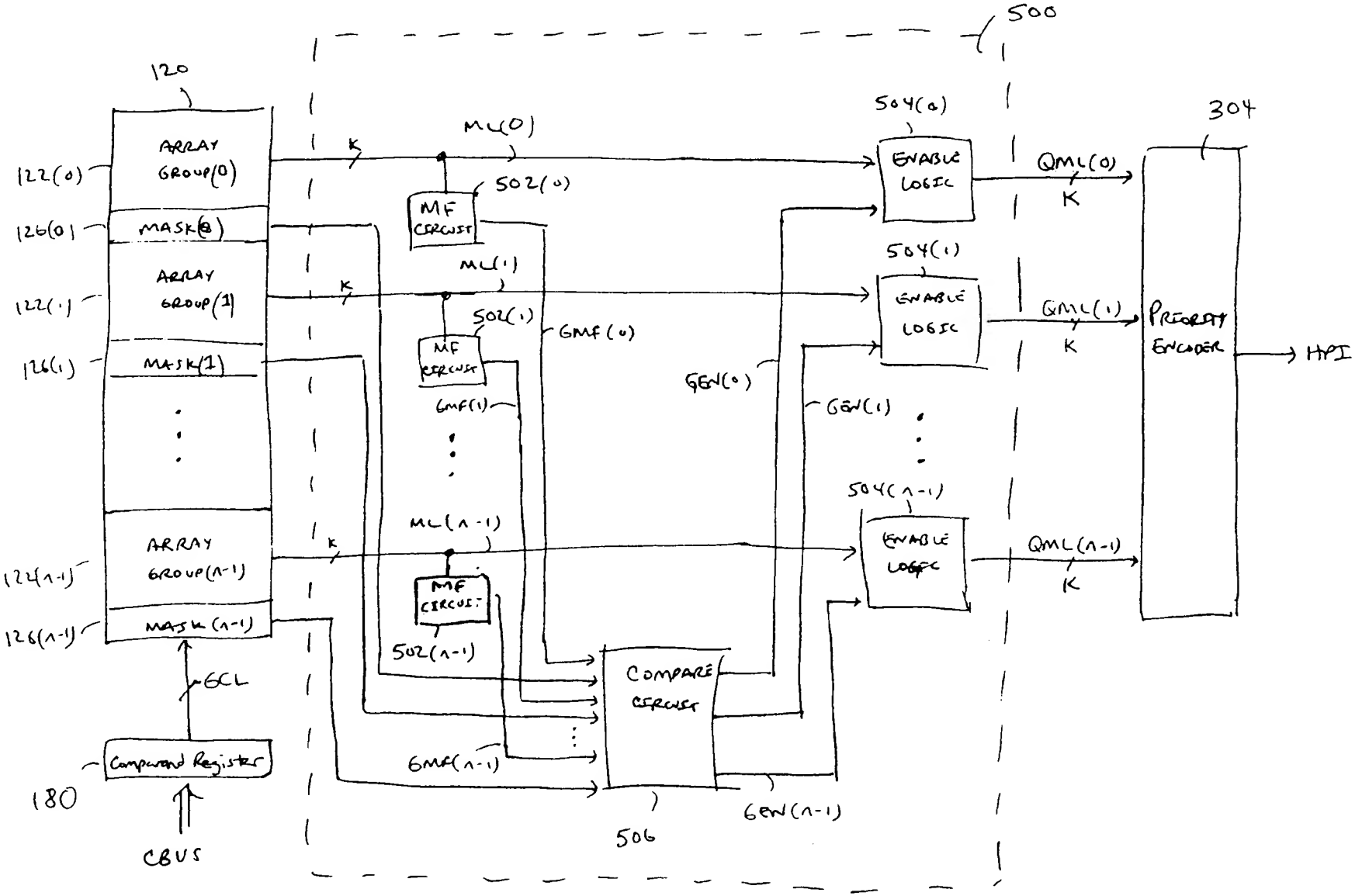
500
120
ARRAY GROUP(0)
ARRAY GROUP(1)
ARRAY GROUP(N-1)
122(0)
126(0)
MASK(0)
122(1)
126(1)
MASK(1)
124(N-1)
126(N-1)
MASK(N-1)
K
ML(0)
ML(1)
ML(N-1)
MF CIRCUIT
502(0)
502(1)
502(N-1)
GMF(0)
GMF(1)
GMF(N-1)
GCL
Command Register
180
CBUS
COMPARE CIRCUIT
506
GEN(0)
GEN(1)
GEN(N-1)
504(0)
504(1)
504(N-1)
ENABLE LOGIC
QML(0)
QML(1)
QML(N-1)
304
PRIORITY ENCODER
HPI

FIG. 5A

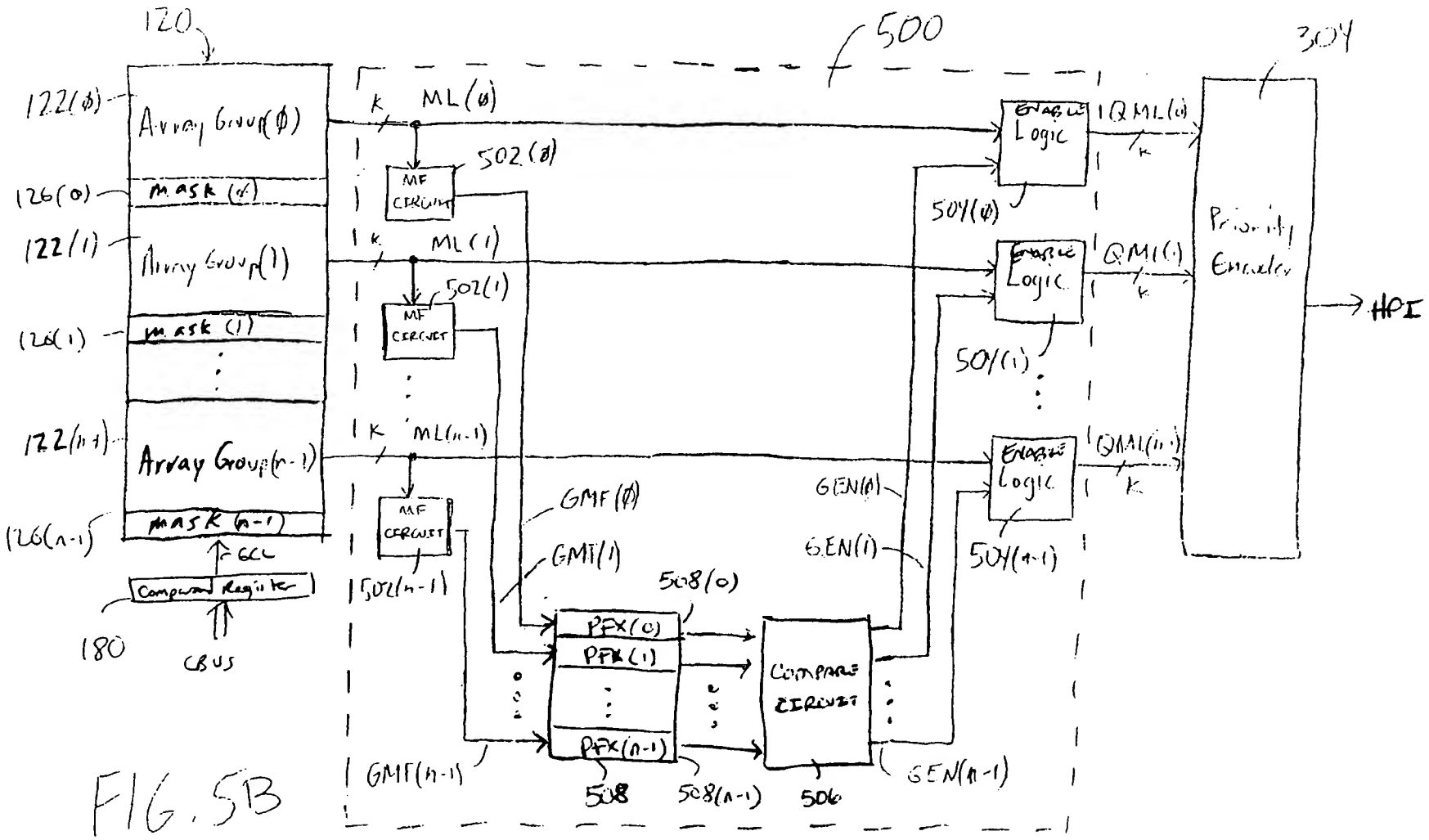

FIG. 5B

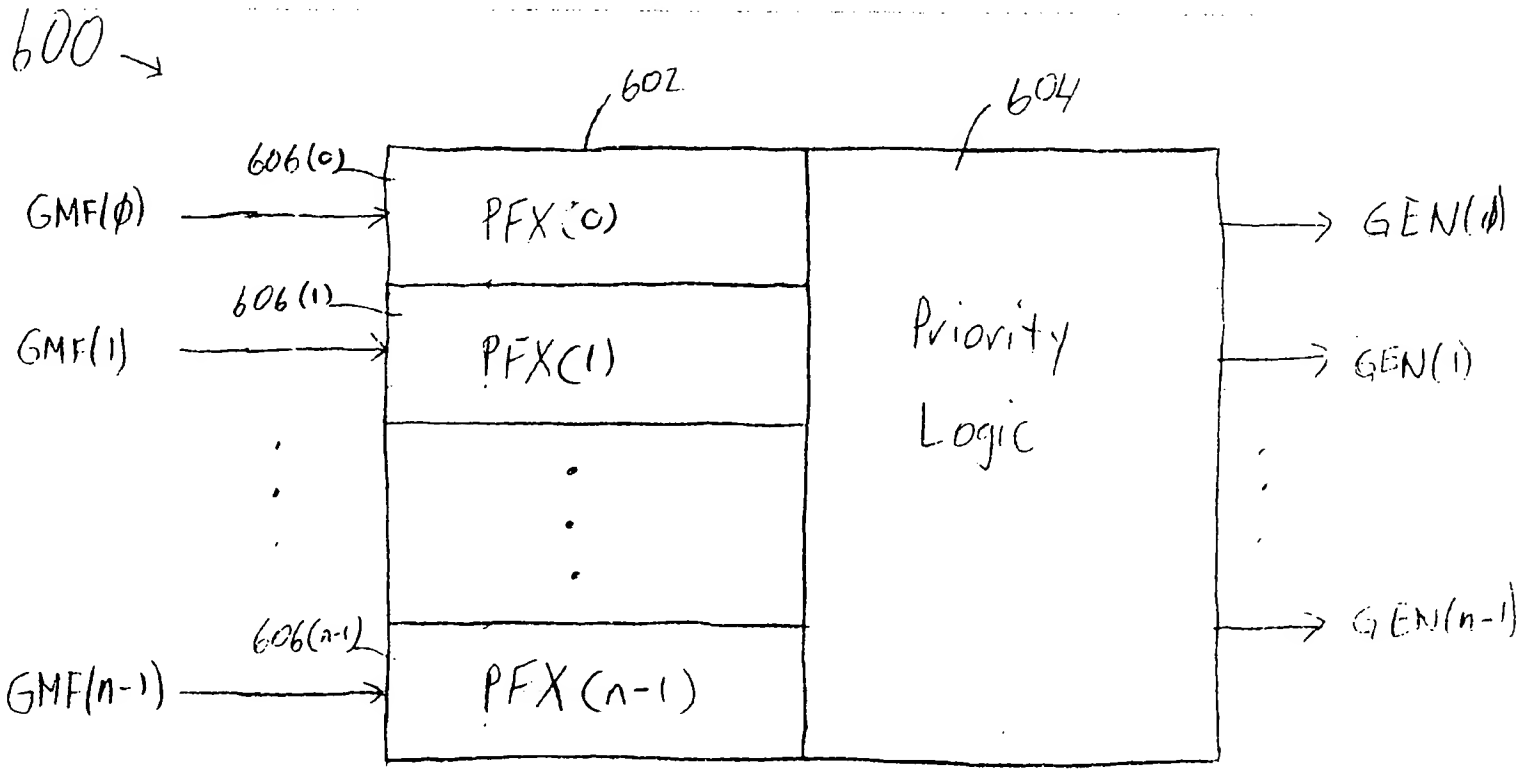

FIG. 6

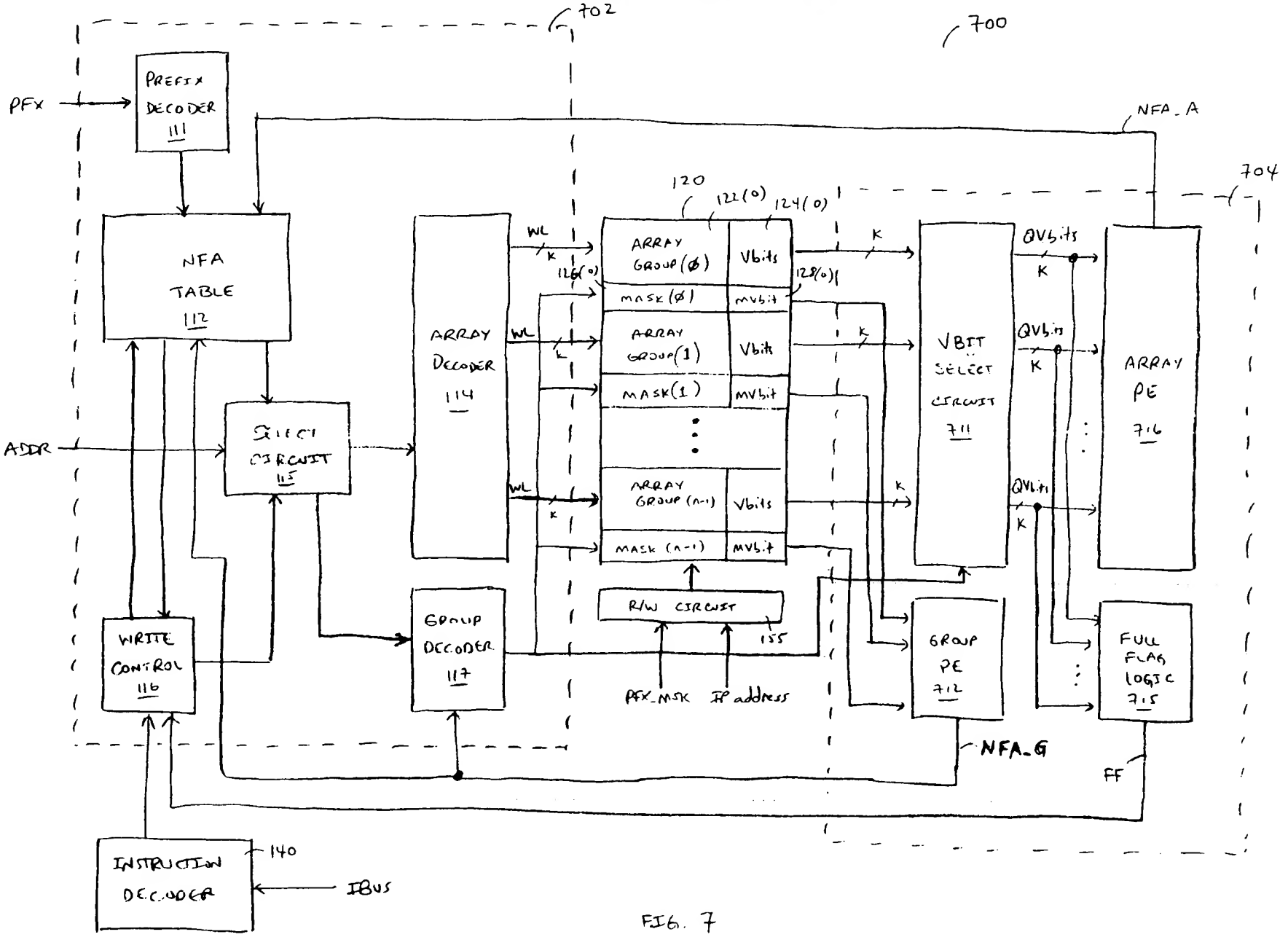
702
700
PFX
PREFIX DECODER 111
NFA_A
704
120
122(0)
124(0)
NFA TABLE 112
ADDR
SELECT CIRCUIT 115
ARRAY DECODER 114
WL
K
126(0)
128(0)
ARRAY GROUP(Ø)
Vbits
MASK(Ø)
MVbit
ARRAY GROUP(1)
MASK(1)
ARRAY GROUP(n-1)
MASK(n-1)
VBIT SELECT CIRCUIT 711
QVbits
ARRAY PE 716
WRITE CONTROL 116
GROUP DECODER 117
R/W CIRCUIT
155
PFX_MSK
IP address
GROUP PE 712
FULL FLAG LOGIC 715
NFA_G
FF
INSTRUCTION DECODER
140
IBUS

FIG. 7

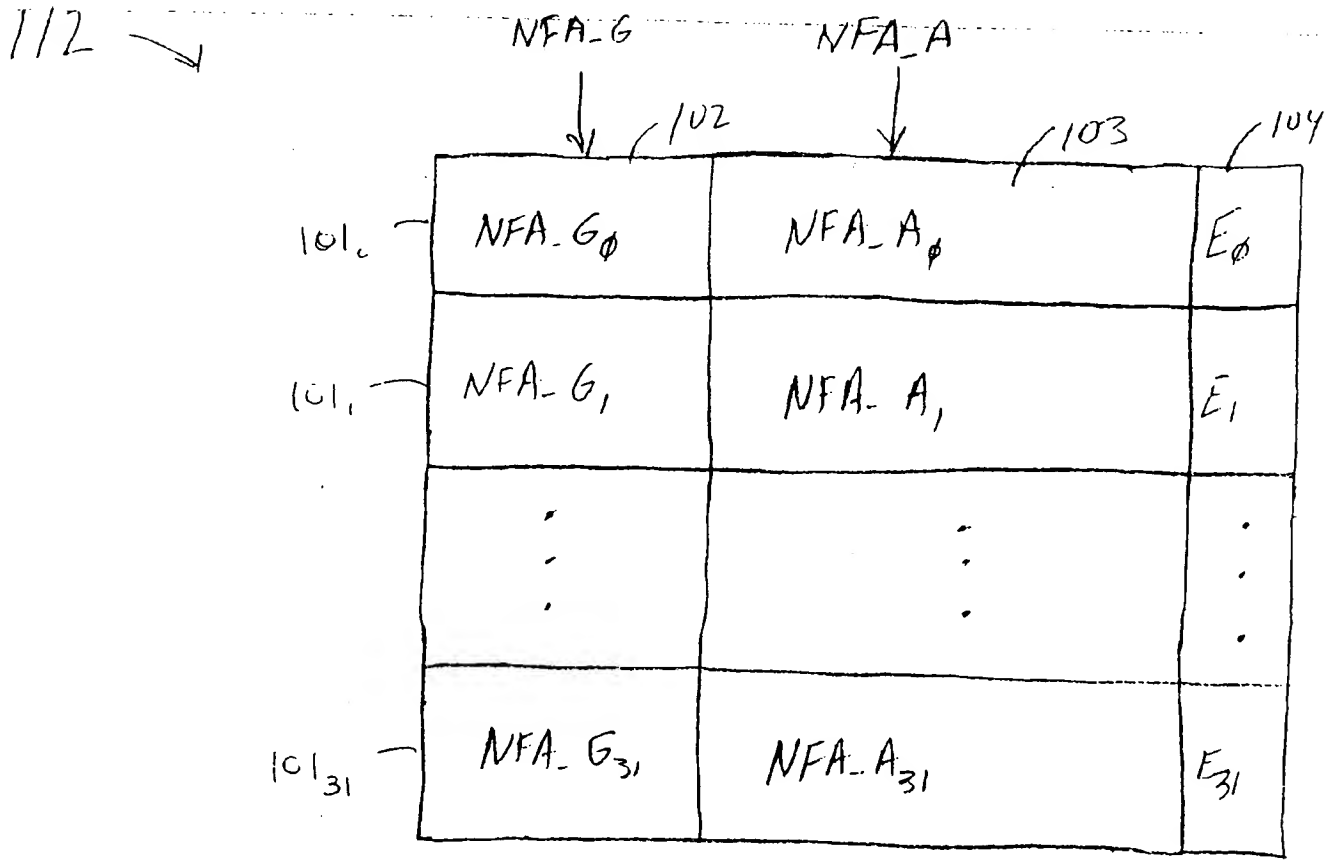

FIG. 8

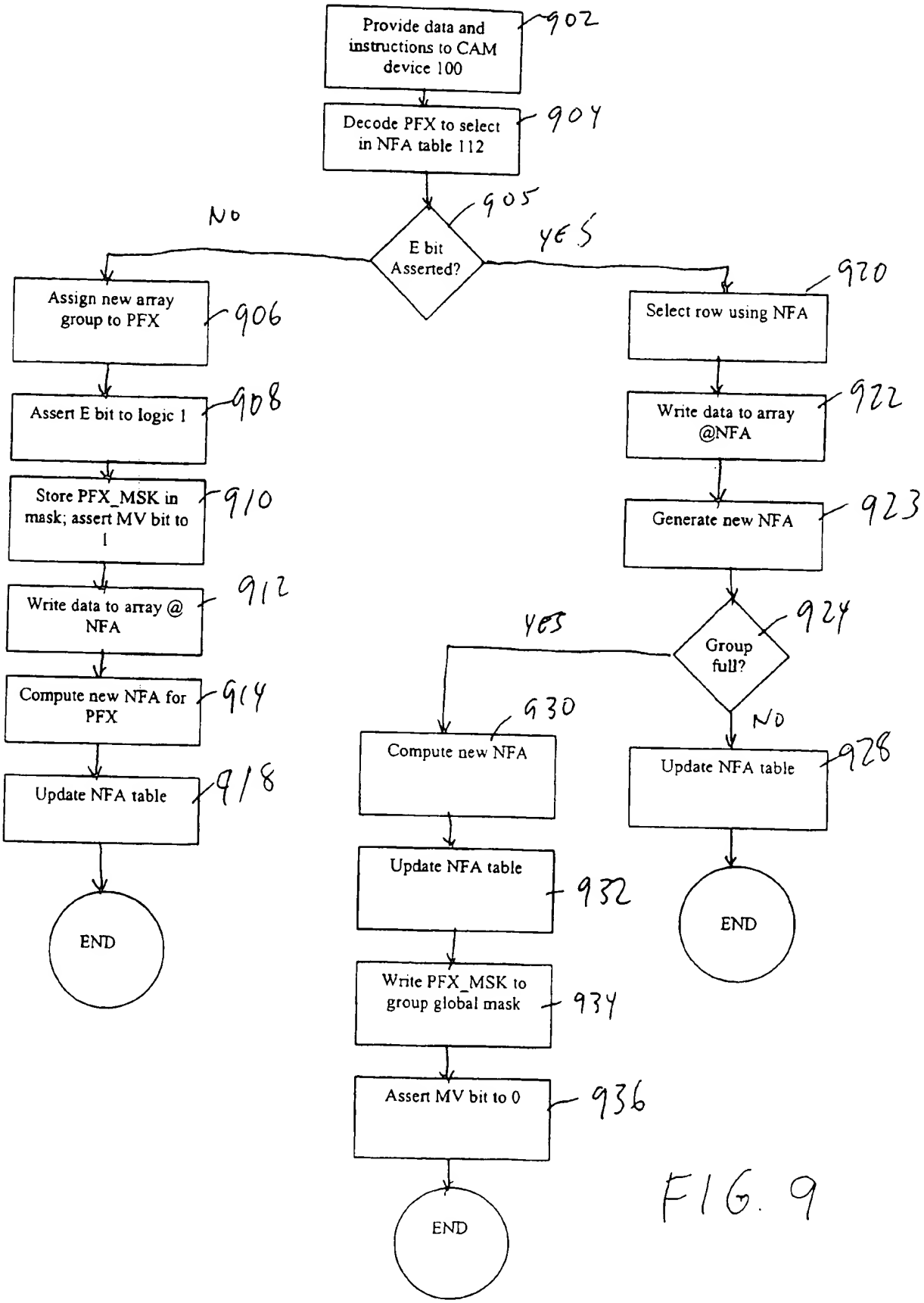
Provide data and instructions to CAM device 100
902
Decode PFX to select in NFA table 112
904
E bit Asserted?
905
No
Yes
Assign new array group to PFX
906
Assert E bit to logic 1
908
Store PFX_MSK in mask; assert MV bit to 1
910
Write data to array @ NFA
912
Compute new NFA for PFX
914
Update NFA table
918
END
Select row using NFA
920
Write data to array @NFA
922
Generate new NFA
923
Group full?
924
Yes
No
Compute new NFA
930
Update NFA table
932
Write PFX_MSK to group global mask
934
Assert MV bit to 0
936
END
Update NFA table
928
END

FIG. 9

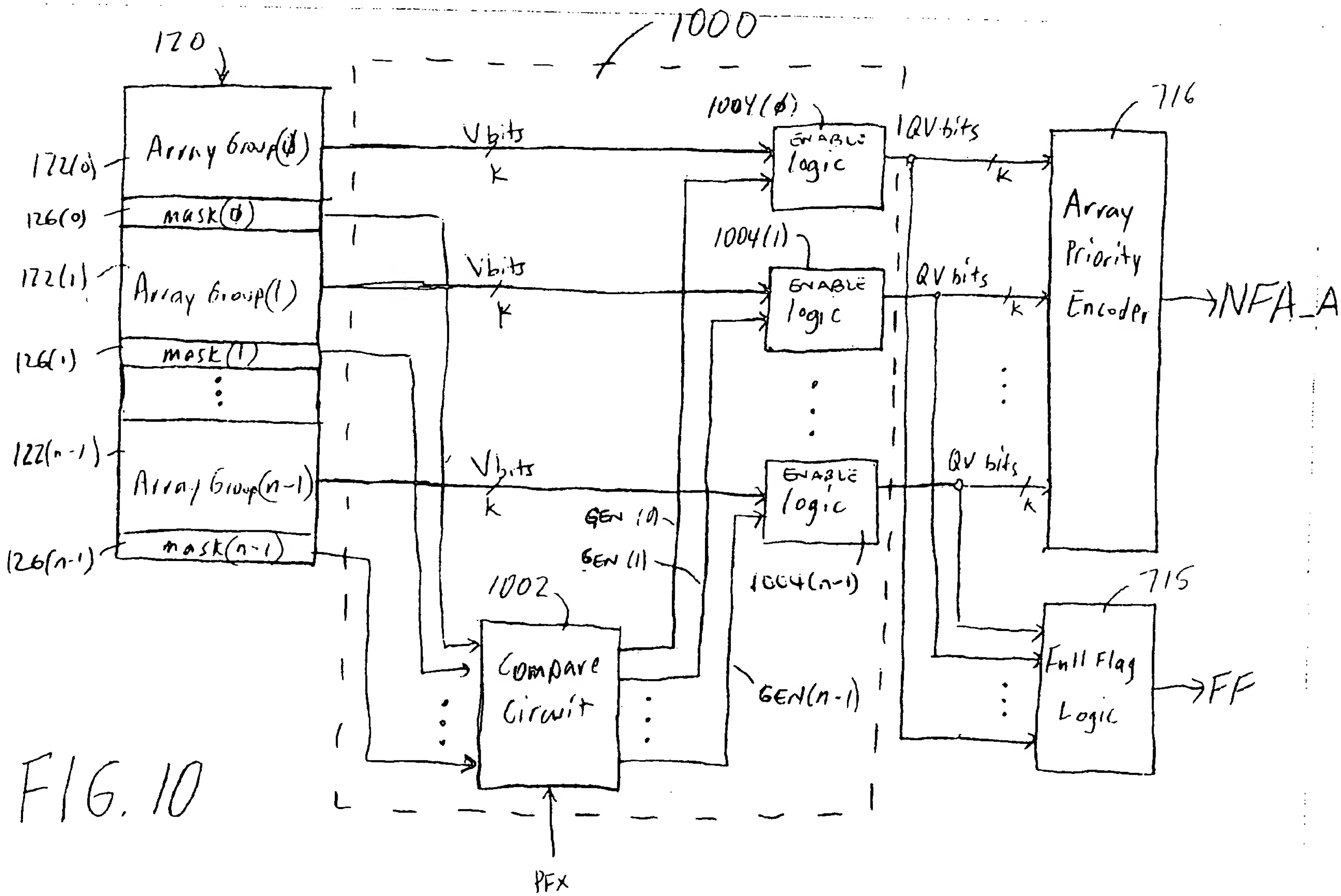
1000
120
Array Group(0)
mask(0)
Array Group(1)
mask(1)
Array Group(n-1)
mask(n-1)
122(0)
126(0)
122(1)
126(1)
122(n-1)
126(n-1)
Vbits
k
1004(0)
1004(1)
1004(n-1)
ENABLE logic
QV bits
716
Array Priority Encoder
NFA_A
715
Full Flag Logic
FF
GEN(0)
GEN(1)
GEN(n-1)
1002
Compare Circuit
PFX

FIG. 10

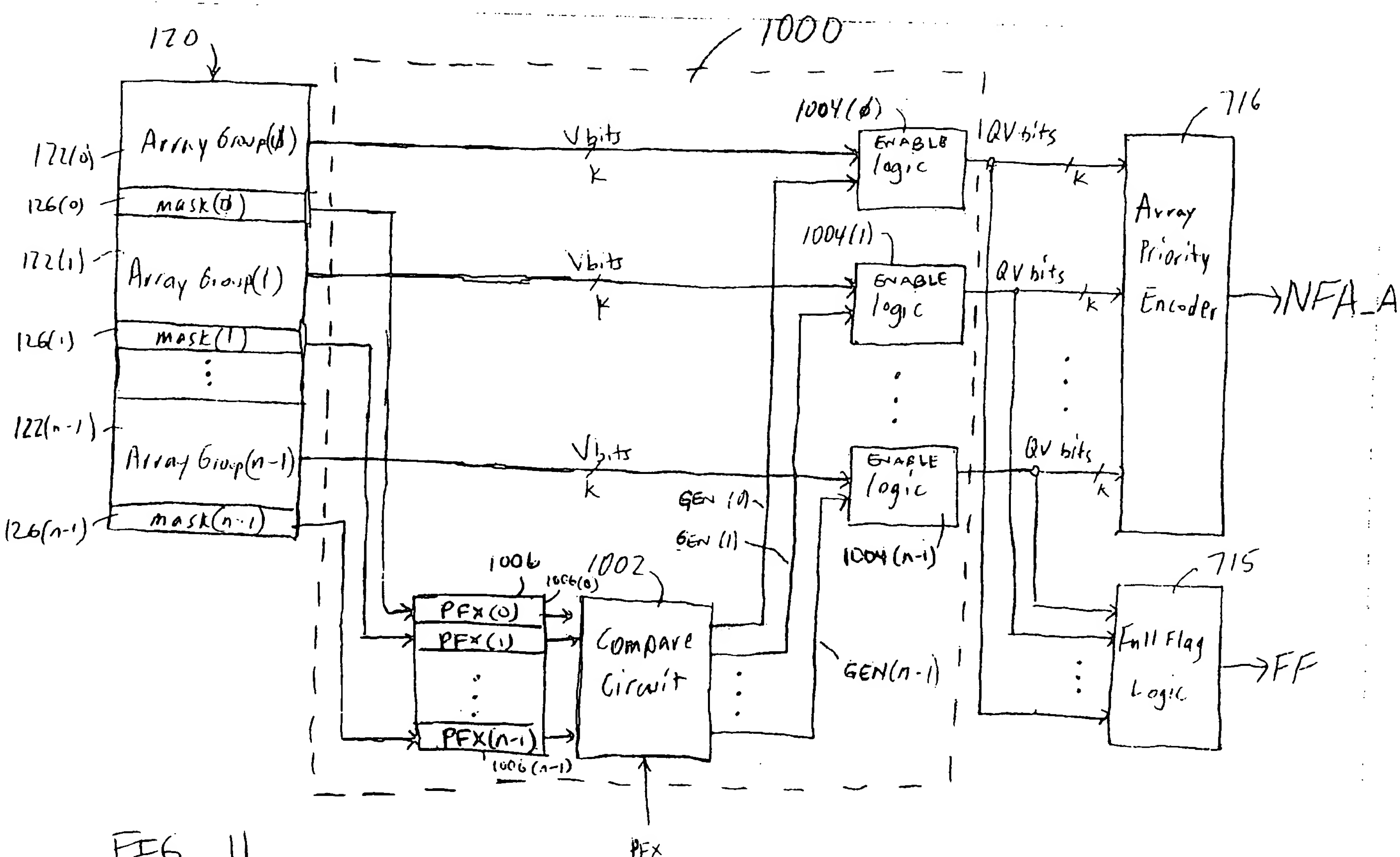
1000
120
122(0)
126(0)
122(1)
126(1)
122(n-1)
126(n-1)
Array Group(0)
mask(0)
Array Group(1)
mask(1)
Array Group(n-1)
mask(n-1)
V bits
k
1004(0)
1004(1)
1004(n-1)
ENABLE logic
1QV bits
QV bits
716
Array Priority Encoder
NFA_A
715
Full Flag Logic
FF
GEN(0)
GEN(1)
GEN(n-1)
1006
1006(0)
1006(n-1)
PFX(0)
PFX(1)
PFX(n-1)
1002
Compare Circuit
PFX

FIG. 11

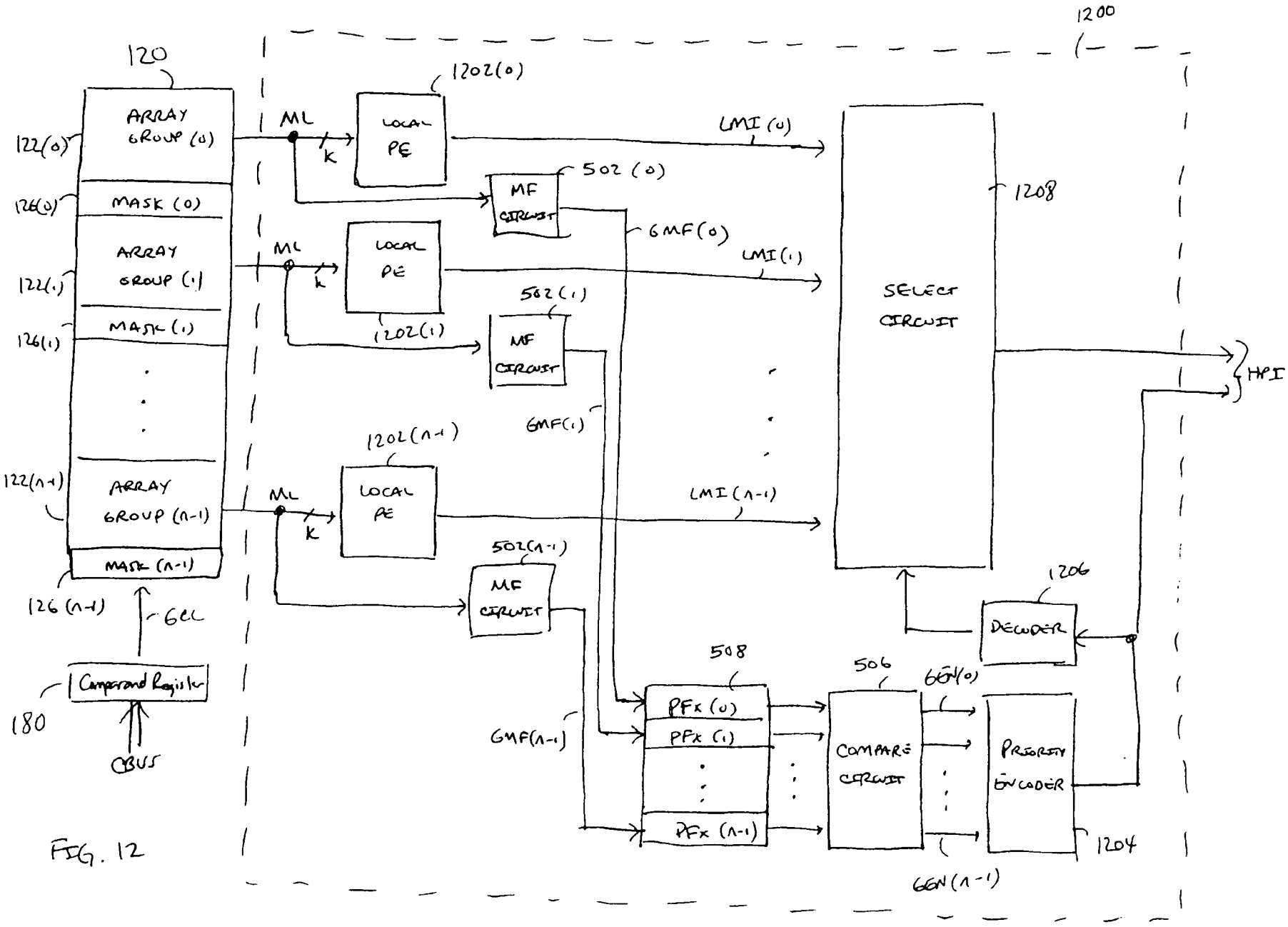
1200
120
ARRAY GROUP (0)
ARRAY GROUP (1)
ARRAY GROUP (n-1)
MASK (0)
MASK (1)
MASK (n-1)
122(0)
122(1)
122(n-1)
126(0)
126(1)
126(n-1)
ML
k
LOCAL PE
1202(0)
1202(1)
1202(n-1)
MF CIRCUIT
502(0)
502(1)
502(n-1)
GMF(0)
GMF(1)
GMF(n-1)
LMI(0)
LMI(1)
LMI(n-1)
SELECT CIRCUIT
1208
HPI
DECODER
1206
GCL
Comparand Register
180
CBUS
508
PEx(0)
PEx(1)
PEx(n-1)
506
COMPARE CIRCUIT
GGN(0)
GGN(n-1)
PRIORITY ENCODER
1204

FIG. 12